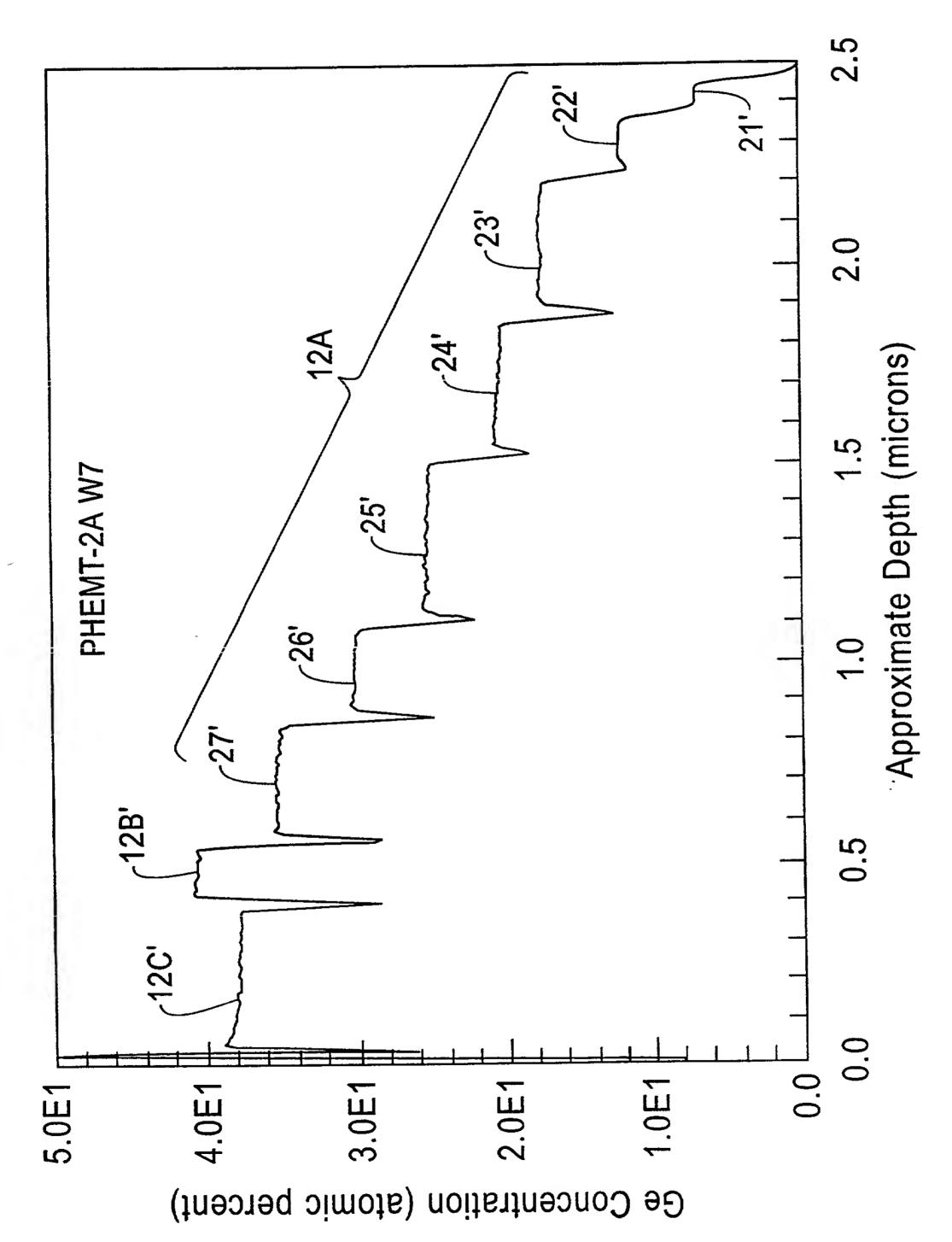
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Fig. 1

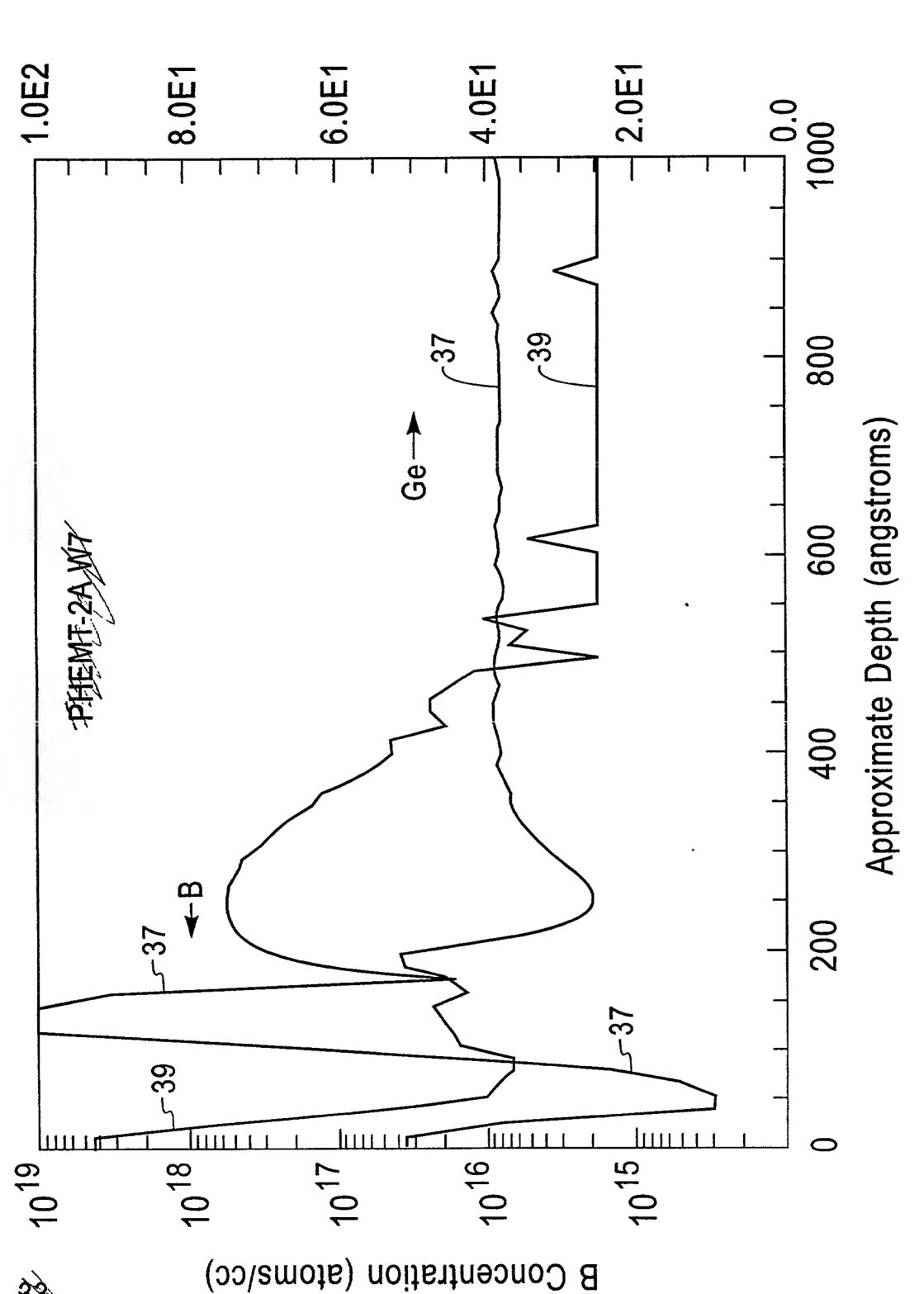
Cap si and SiGe Device Layers Strain Relief Layers Silicon Substrate Thick Buffer (TEM of PHEMT 2.3 Structure 450 nm -11,31 -33 12C -12B 27' 25' 26' 23° 22° 21° 24

Fig. 2



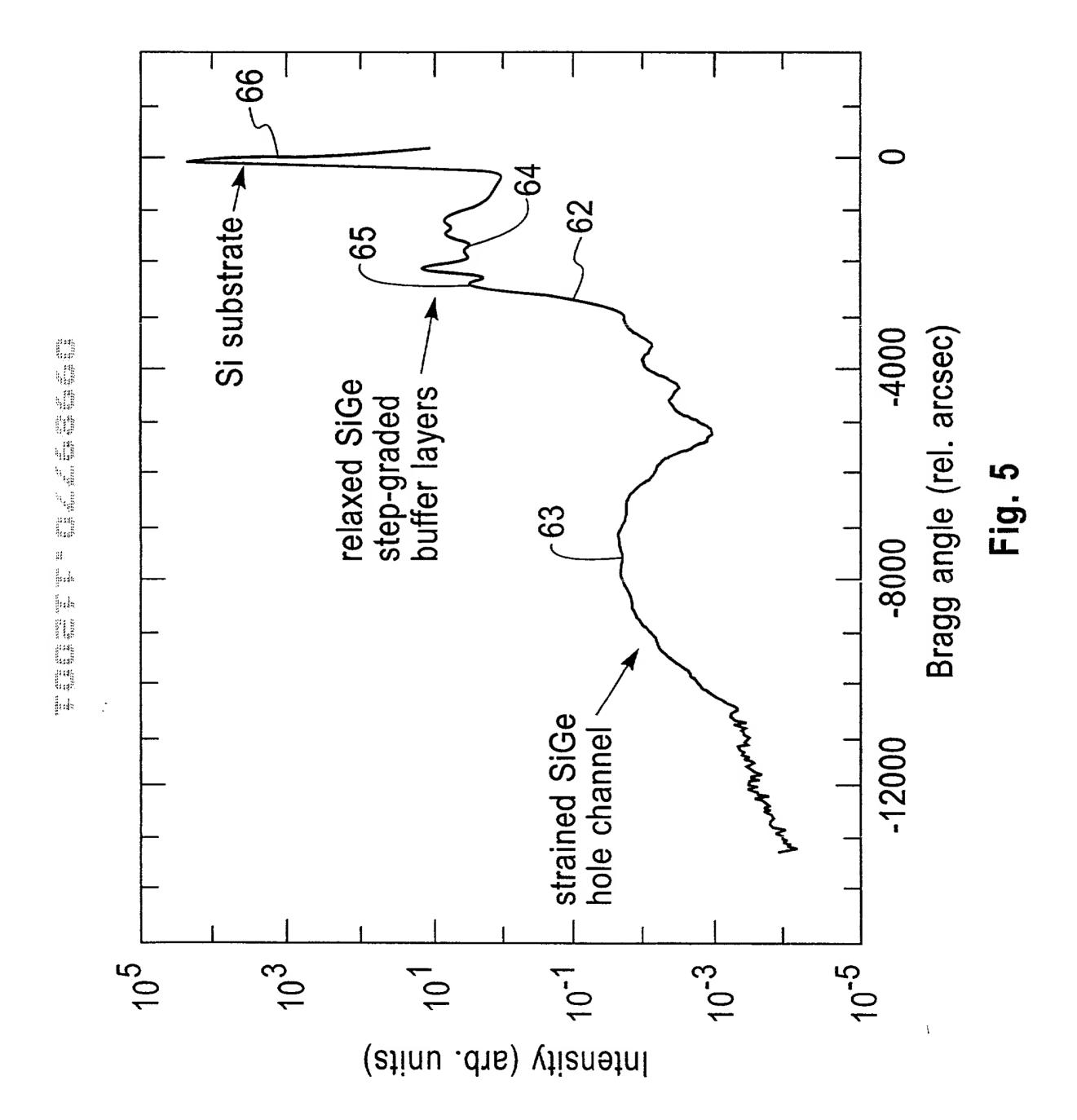
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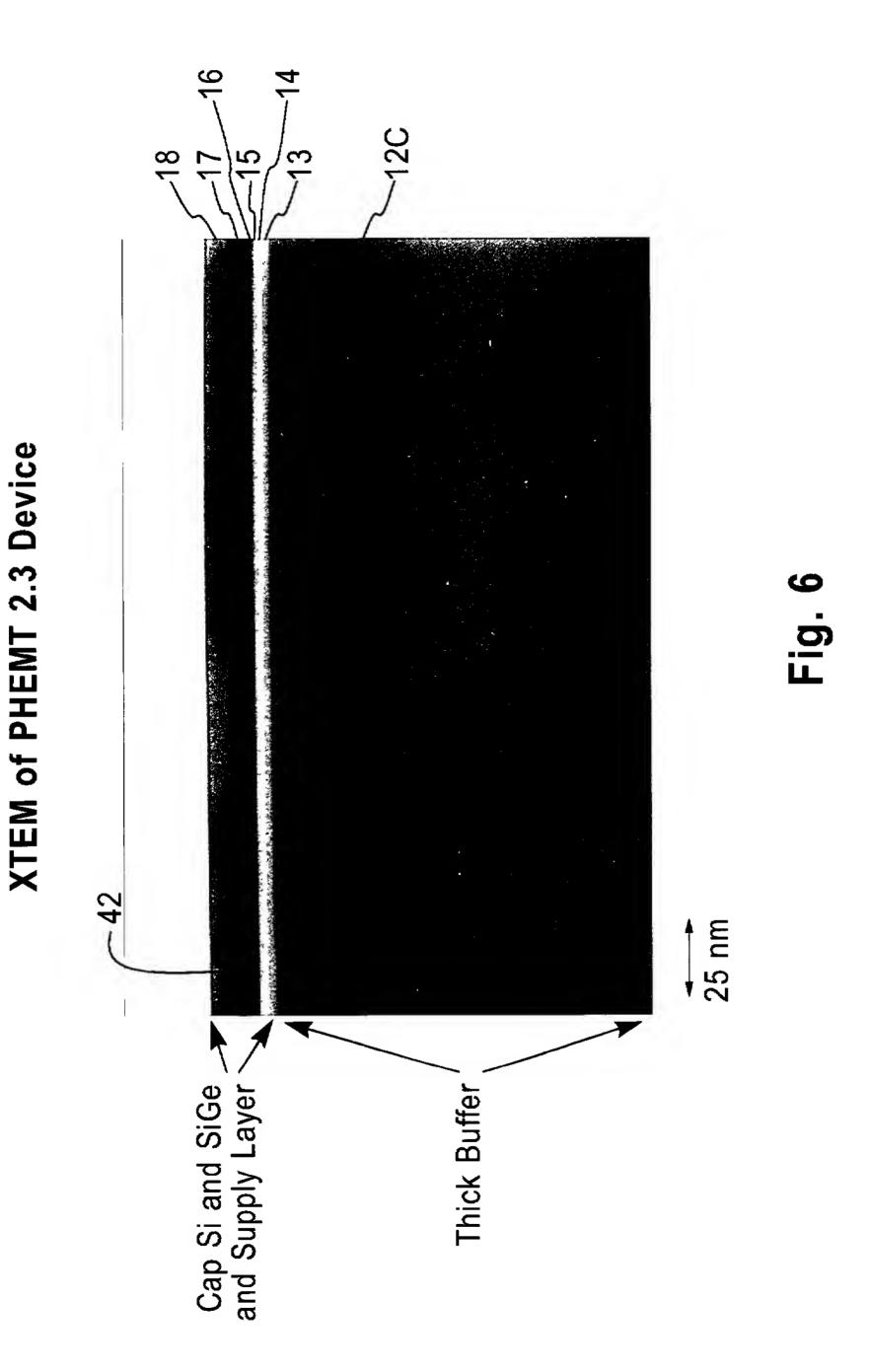
Fig. 3



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Fig. 4

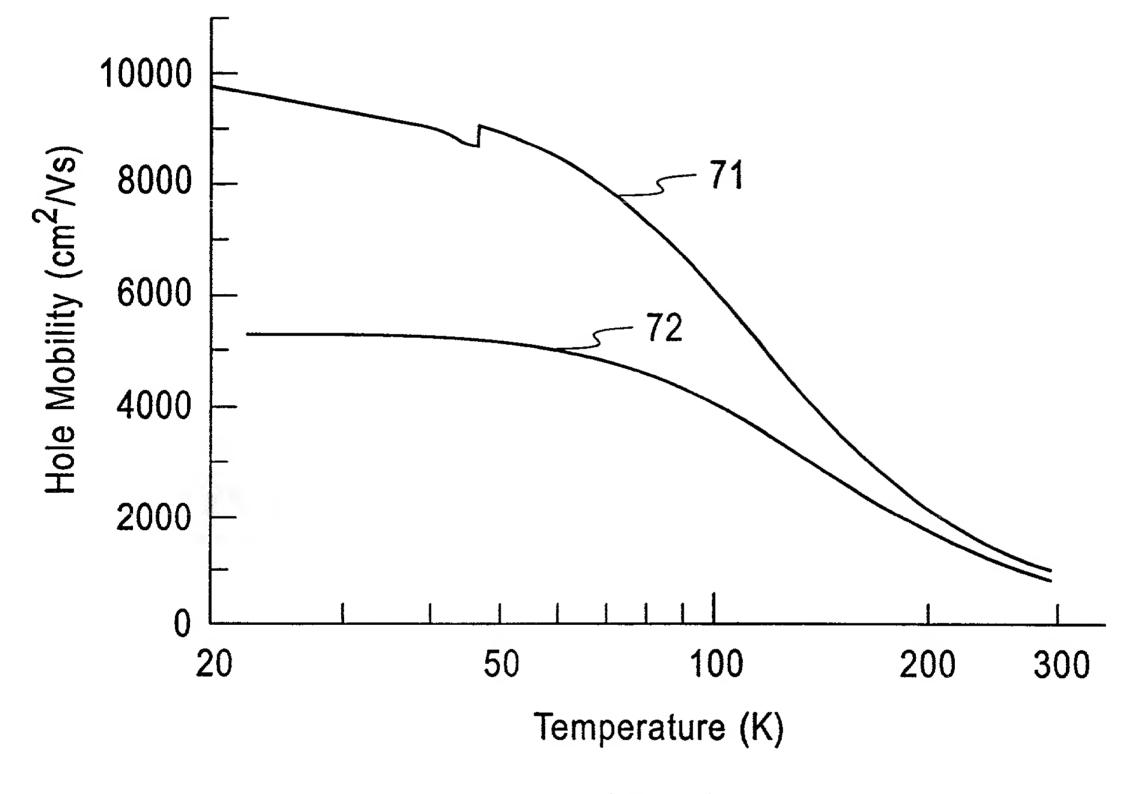




Stacking fault densities ~ 10⁶ - 10⁸/cm²



Fig. 7



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Fig. 8

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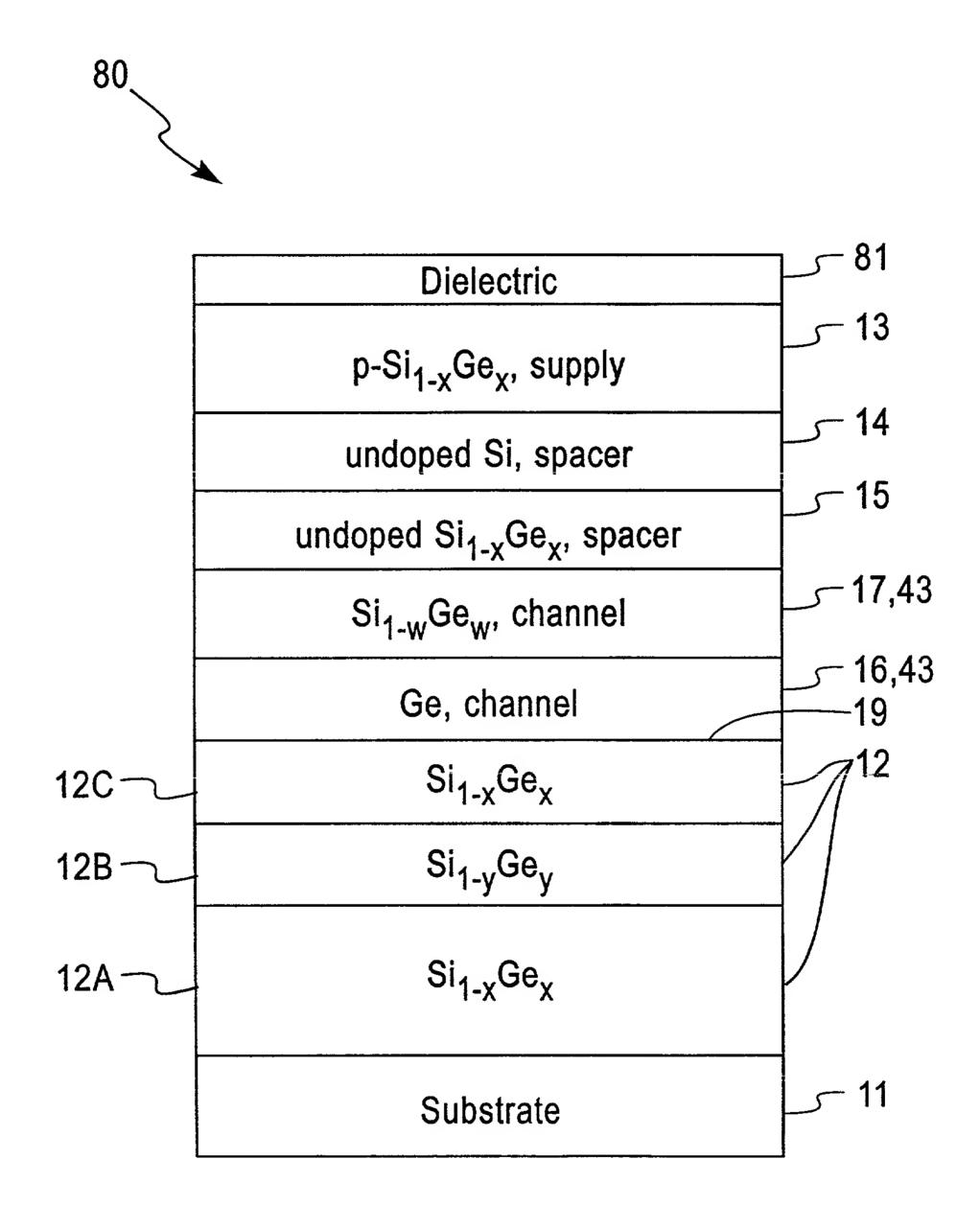
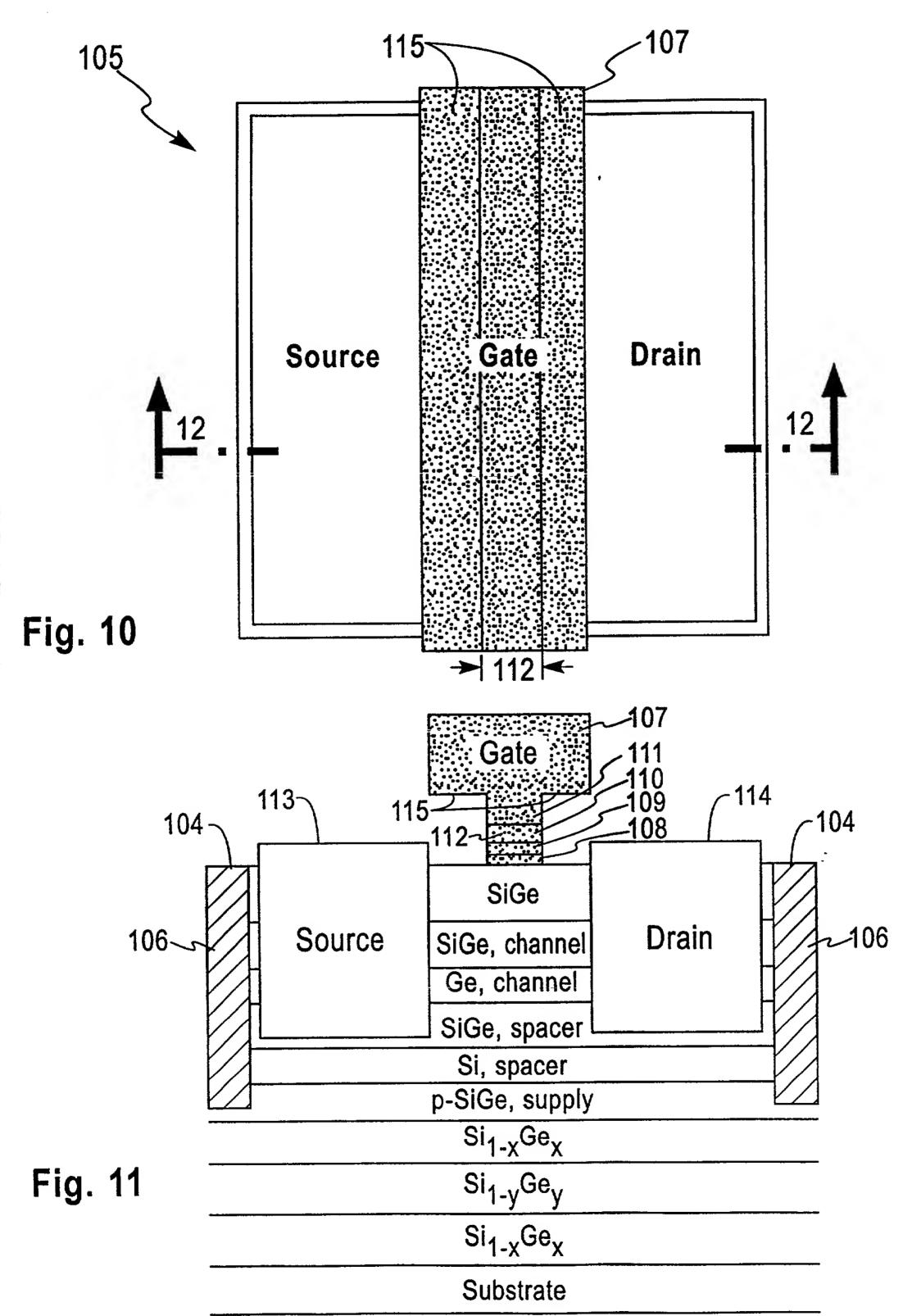


Fig. 9

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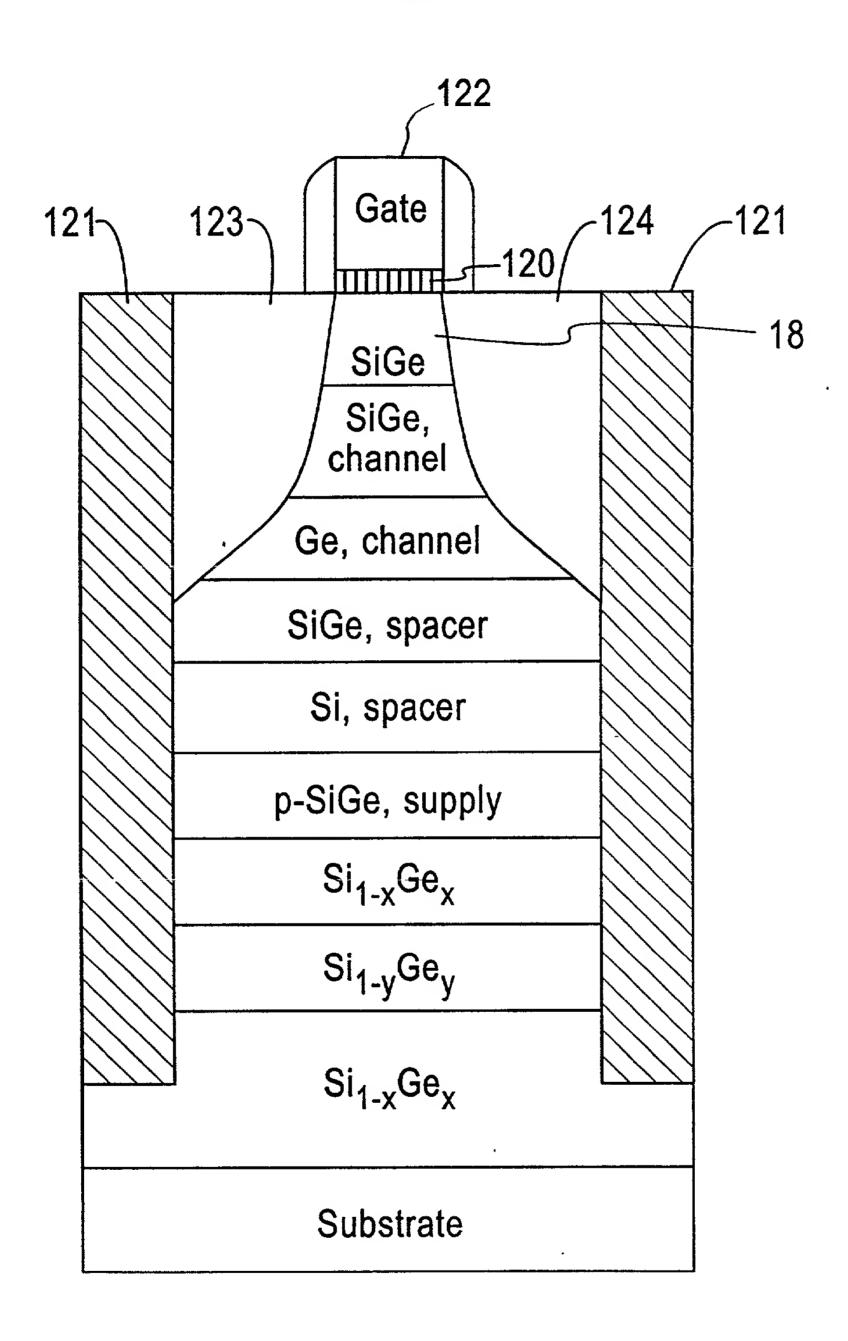


Fig. 12

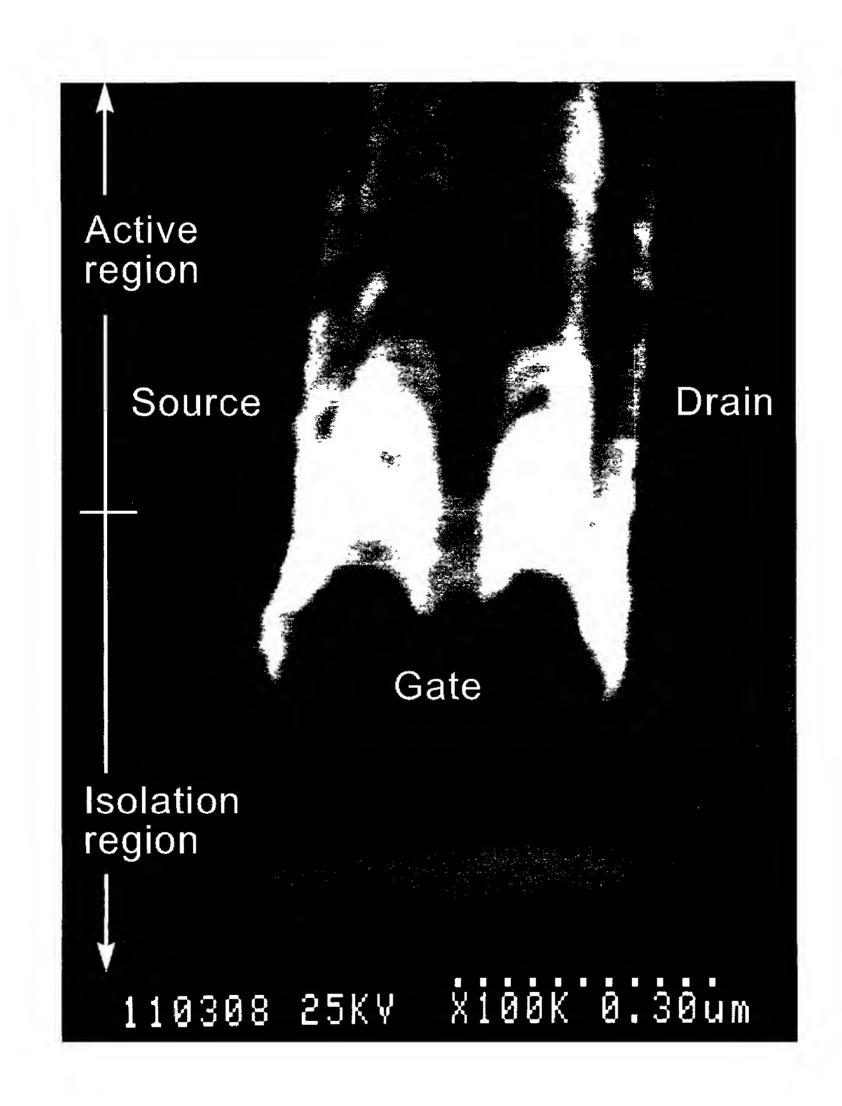


Fig. 13

p-type composite-channel MODFET, L_g = 0.09 μ m, W = 25 μ m

